UNITED STATES PATENT APPLICATION

FOR

METHOD AND APPARATUS FOR PROVIDING MULTIPLE SUPPLY VOLTAGES FOR A PROCESSOR

Inventors:

Kevin X. Zhang
Don J. Nguyen
Daniel J. Lenehan

Prepared by:

David J. Kaplan
Intel Corporation, SC4-202A
2200 Mission College Blvd.
Santa Clara, CA 95052-8119

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The present invention relates to computer systems and more particularly to controlling one or more supply voltages to power one or more circuits of an integrated circuit, such as a processor

BACKGROUND

Computer systems are becoming increasingly pervasive in our society, including everything from small handheld electronic devices, such as personal data assistants and cellular phones, to application-specific electronic components, such as set-top boxes and other consumer electronics, to medium-sized mobile and desktop systems to large workstations and servers. Computer systems typically include one or more processors. A processor manipulates and controls the flow of data in a computer. To provide more powerful computer systems for consumers, processor designers strive to continually increase the operating speed of the processor. Unfortunately, as processor speed increases, the power consumed by the processor tends to increase as well. Historically, the power consumed by a computer system has been limited by two factors. First, as power consumption increases, the computer tends to run hotter, leading to thermal dissipation problems. Second, the power consumed by a computer system may tax the limits of the power supply used to keep the system operational, reducing battery life in mobile systems and diminishing reliability while increasing cost in larger systems.

The present invention addresses this and other problems associated with the prior art.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the accompanying figures in which like references indicate similar elements and in which:

Figure 1 includes a computer system formed in accordance with an embodiment of the present invention;

Figure 2A includes a processor formed in accordance with an embodiment of the present invention;

Figure 2B includes a processor formed in accordance with another embodiment of the present invention;

Figure 2C includes a processor formed in accordance with an alternate embodiment of the present invention;

Figure 3A includes a circuit formed in accordance with an embodiment of the present invention;

Figure 3B includes a circuit formed in accordance with another embodiment of the present invention; and

Figure 4 includes a flow chart showing a method of the present invention.

DETAILED DESCRIPTION

In accordance with an embodiment of the present invention, a processor may include analog circuitry including one or more op amps. For one embodiment of the present invention, the op amp may be in a differential configuration including an input coupled to a supply voltage, Vcc, provided by an external voltage regulator. In

this manner, the op amp may be part of a voltage sensor, the output of the op amp being a control signal to indicate if the supply voltage is above or below a target value. This target value may be adjusted by the processor in accordance with a power management policy. The control signal may be provided to the external voltage regulator to adjust the supply voltage accordingly.

For this or another embodiment of the present invention, an op amp may form a portion of an integrated voltage regulator, the op amp being powered by an external voltage regulator and generating a local supply voltage for the processor. This local supply voltage may be set to allow a circuit powered by the local supply voltage to meet a timing requirement. The local supply voltage may be adjusted by the processor in accordance with a power management policy. In accordance with one embodiment of the present invention, the processor may include multiple integrated voltage regulators generating multiple local supply voltages. Each local supply voltage may be independently adjusted to allow corresponding circuits to meet timing requirements and for power management.

A more detailed description of embodiments of the present invention, including various configurations and implementations, is provided below.

Figure 1 includes a computer system that may be formed in accordance with an embodiment of the present invention. As shown, the computer system may include a processor 100 coupled to hub 110. Processor 100 may be powered by one or more voltages from voltage regulator 150. Processor 100 may communicate with graphics controller 105, main memory 115, and hub 125 via hub 110. Hub 125 may couple peripheral device 120, storage device 130, audio device 135, video

device 145, and bridge 140 to hub 110. Bridge 140 may couple hub 125 to one or more additional buses coupled to one or more additional peripheral devices. Note that in accordance with alternate embodiments of the present invention, a computer system may include more or fewer components than those shown in Figure 1. Note, also, that the components of Figure 1 may be partitioned differently. For example, multiple components may be integrated into a single component, and single components may be divided into multiple components.

For one embodiment of the present invention, voltage regulator 150 is a discrete voltage regulator that is external to processor 100 of Figure 1. Voltage regulator 150 may provide one or more supply voltages to processor 100 alone or in addition to providing one or more supply voltages to other components of the computer system. In addition, there may be one or more additional voltage regulators that provide one or more additional supply voltages to processor 100. Note that the term "Vcc" may be used herein to denote a supply voltage.

Although embodiments of the present invention may be described herein in association with a processor, it is to be noted that embodiments of the present invention may be implemented in other components as well. Therefore, for convenience, the term "processor" may be used herein to refer not only to a processor (e.g. a central or multi-processing unit, digital signal processor, micro-controller, etc.) but also to other components such as a hub (e.g. a bridge, chipset, etc.) or a controller (e.g. a graphics controller, memory controller, etc).

In accordance with one embodiment of the present invention, processor 100 and voltage regulator 150 of Figure 1 may be implemented as processor 200 and

voltage regulator 205 of Figure 2A. Voltage regulator 205 provides a supply voltage, Vcc, to processor 200 via one or more voltage/power supply lines that couple voltage regulator 205 to one or more supply voltage input ports of processor 200. This Vcc may be distributed to various circuits of processor 200 to power the circuits. In addition, processor 200 includes a voltage sensor 201 coupled to one or more supply voltage input ports of processor 200 to receive Vcc. Voltage sensor 201 monitors Vcc received from the voltage regulator and, in response, provides a control signal to indicate if the supply voltage is above or below a target value. The control signal may be provided back to voltage regulator 205 via one or more control signal lines that couple one or more control signal ports of processor 200 to voltage regulator 205.

Based on the control signal from voltage sensor 201 of Figure 2A, voltage regulator 205 may adjust Vcc higher or lower to achieve the target value as measured by the voltage sensor. During normal operation (e.g. when the processor is in a wake/active state, executing instructions), Vcc may be set to a target value that allows the processor, or a portion thereof, to meet a timing requirement at a given frequency. This target value may be adjusted by the processor in accordance with a power management policy. For example, when the processor is in a sleep/inactive state, the target value may be reduced by the processor. As another example, the target value may be adjusted in response to a change in the operating frequency of the processor.

By including voltage sensor 201 as part of the same integrated circuit as processor 200, the accuracy of Vcc monitoring may be improved in comparison to

integrating the voltage sensor with voltage regulator 205 of Figure 2A. One reason for this improved accuracy is that monitoring the supply voltage at the processor rather than at the voltage regulator may reduce Vcc variation due to, for example, variation in voltage/power supply line routings between the voltage regulator and the processor. Increased accuracy of Vcc monitoring may improve the ability to implement tighter Vcc design margins. Tighter Vcc design margins may lead to a reduction in Vcc, resulting in a reduction of the overall power consumed by the processor.

Voltage sensor 201 of Figure 2A may be designed using one or more op amps, comparators, or switching regulators that may include analog circuits integrated with the digital circuitry of processor 200 together on the same semiconductor substrate (i.e. as a single integrated circuit). An op amp of voltage sensor 201 may be designed in a differential or comparator configuration, such as the circuit of Figure 3A, to be described in more detail below. In accordance with one embodiment of the present invention, multiple voltage sensors may be integrated on the same semiconductor substrate as the processor.

In accordance with one embodiment of the present invention, processor 100 and voltage regulator 150 of Figure 1 may be implemented as processor 210 and voltage regulator 215 of Figure 2B. Voltage regulator 215 provides a supply voltage, Vcc(global), to processor 210 via one or more voltage/power supply lines that couple voltage regulator 215 to one or more supply voltage input ports of processor 210. Processor 200 includes a local voltage regulator 211 coupled to one or more supply voltage input ports of processor 210 to receive Vcc(global). Voltage

regulator 211 may be powered by Vcc(global) and provides a local supply voltage Vcc(local) for the processor. This Vcc(local) may be distributed to various circuits of processor 210 to power the circuits. In addition, Vcc(global) may also be distributed to various circuits of processor 210 to power the circuits. For example, Vcc(local) may be used to power all or a portion of a core of processor 210, and Vcc(global) may be used to power all or a portion of an input/output ring of processor 210. In accordance with one embodiment of the present invention, Vcc(local) may be less than Vcc(global).

The local supply voltage, Vcc(local), provided by voltage regulator 211 of Figure 2B may be adjusted by processor 210 in control of voltage regulator 211. During normal operation (e.g. when the processor is in a wake/active state, executing instructions), Vcc(local) may be set to a value that allows the processor, or a portion thereof, to meet a timing requirement at a given frequency. This value may be adjusted by the processor in accordance with a power management policy. For example, when the processor is in a sleep/inactive state, Vcc(local) may be reduced by the processor. As another example, the Vcc(local) may be adjusted in response to a change in the operating frequency of the processor.

By including voltage regulator 211 as part of the same integrated circuit as processor 210, two or more different supply voltages can be routed to the various circuits of the processor. By providing processor 210 with different supply voltages at different voltage levels, each supply voltage can be individually tuned to the circuitry that it powers, resulting in a reduction of the overall power consumed by the processor.

Voltage regulator 211 of Figure 2B may be designed using one or more op amps, comparators, or switching regulators that may include analog circuits integrated with the digital circuitry of processor 200 together on the same semiconductor substrate. An op amp of voltage regulator 211 may be designed as described below in conjunction with Figure 3B. In accordance with one embodiment of the present invention, multiple voltage regulators may be integrated on the same semiconductor substrate as the processor. For another embodiment of the present invention, one or more voltage regulators may be integrated with one or more voltage sensors on the same semiconductor substrate as the processor.

In accordance with one embodiment of the present invention, processor 100 and voltage regulator 150 of Figure 1 may be implemented as processor 250 and voltage regulator 270 of Figure 2C. Voltage regulator 270 provides a supply voltage, Vcc(global), to processor 250 via one or more voltage/power supply lines that couple voltage regulator 270 to one or more supply voltage input ports of processor 250. Processor 250 includes a global power grid 280 coupled to one or more supply voltage input ports of processor 250 to receive Vcc(global). Global power grid 280 may distribute Vcc(global) throughout the processor and, in particular, to multiple local voltage regulators 251-254.

Each local voltage regulator 251-254 of Figure 2C may be powered by Vcc(global) via global power grid 280, and each provides a local supply voltage, Vcc(local), for the processor. Each Vcc(local) may be distributed via a local power grid to a circuit of processor 250 to power the circuit. For example, local voltage regulator 251 is powered by Vcc(global) via global power grid 280 and provides

Vcc(local) to power circuit 261 via local power grid 285. Similarly, local voltage regulators 252-254 are powered by Vcc(global) via global power grid 280 and provide independent local supply voltages to power circuits 262-264, respectively, via local power grids 286-288, respectively.

Each local supply voltage provided by each local voltage regulator 251-254 of Figure 2C may be independently adjusted by processor 250. During normal operation (e.g. when the associated circuit is active), each Vcc(local) may be set to a value that allows the associated circuit, or a portion thereof, to meet a timing requirement at a given frequency. These values may be adjusted by the processor in accordance with a power management policy. For example, when a circuit powered by a local voltage regulator is inactive, the local supply voltage provided by the local voltage regulator may be reduced by the processor. The local supply voltage may additionally be adjusted in response to a change in the operating frequency of the processor.

As one example, a circuit, such as circuit 261 of Figure 2C, powered by a local supply voltage provided by a local voltage regulator, such as local voltage regulator 251, may be a branch prediction unit of the processor. When the branch prediction unit is active (e.g. when the unit is processing a branch instruction) the local supply voltage that powers the branch prediction unit may be set to a value that allows the unit to meet a minimum timing requirement at the frequency of operation. When the branch prediction unit is inactive (e.g. between branch instructions), the local supply voltage may be reduced. Similarly, a separate circuit, such as circuit 262, powered by a local supply voltage provided by a local voltage

regulator, such as local voltage regulator 252, may be a floating point unit of the processor. When the floating point unit is active (e.g. when the unit is processing a floating point instruction) the local supply voltage that powers the floating point unit may be set to a value that allows the unit to meet a minimum timing requirement at the frequency of operation. When the floating point unit is inactive (e.g. between floating point instructions), the local supply voltage may be reduced.

In this manner, local voltage regulators may provide local supply voltages at different voltage levels to different circuits of the processor. Each local supply voltage can be individually tuned to the circuitry that it powers. For example, the local supply voltage that powers a critical, high performance circuit may be set to a higher voltage than the local supply voltage that powers a less critical, lower performance circuit. This may enable both circuits to meet their timing requirements at the lowest (or nearly the lowest) local supply voltage appropriate for the each circuit individually. This may result in a reduction of the overall power consumed by the processor.

For an alternate embodiment of the present invention, circuits 261-264 may be any other functional unit or other circuit of processor 250 of Figure 2C. For one embodiment, one or more circuits of circuits 261-264 may be all or a portion of one or more processor cores or memory regions such as a cache. In addition, in accordance with an embodiment of the present invention, a processor may include any number of local voltage regulators, each providing a Vcc(local) to power any number of circuits of the processor.

Voltage regulators 251-254 of Figure 2C may be designed using one or more op amps, comparators, or switching regulators that may include analog circuits integrated with the digital circuitry of processor 250 together on the same semiconductor substrate. An op amp of voltage regulators 251-254 may be designed as described below in conjunction with Figure 3B.

Figure 3A includes an op amp in a differential configuration formed in accordance with an embodiment of the present invention. Output 325 of op amp 300 is fed back to the inverting input of the op amp via resistor 315, and the input voltage 320 is provided to the inverting input of the op amp via resistor 310. The input voltage 330 is provided to the non-inverting input of op amp 300 via resistor 335, and the non-inverting input of the op amp is coupled to ground (or Vss) via resistor 340. Resistors 310, 315, 335, and 340 are digitized resistors, the resistances of which may be set by values entered into control register 305 (which may be implemented as a single or multiple registers). The processor with which the circuit of Figure 3A may be integrated may set the values in control register 305 to control the output at 325.

In accordance with an embodiment of the present invention in which the circuit of Figure 3A is used as a voltage sensor, a stable reference voltage, Vref, may be provided as input voltage 320. Vcc (or the voltage to be sensed) may be provided as input voltage 330, and the control signal may be provided at output 325. The resistance of resistor 315 may be kept equal to the resistance of resistor 340, and the resistance of resistor 310 may be kept equal to the resistance of resistor 335. Under these circumstances, the control signal provided at output 325 may be

determined by the equation 315/310 x (Vcc – Vref) where 315 and 310 are the resistances of resistors 315 and 310, respectively.

Figure 3B includes a circuit formed in accordance with an embodiment of the present invention. Output 360 of op amp 350 is fed back to the inverting input of the op amp via resistor 375, and the inverting input of the op amp is coupled to ground (or Vss) via resistor 370. Input voltage 365 is provided to the non-inverting input of op amp 350. Supply voltage 355 is provided to power the circuit. Resistors 370 and 375 are digitized resistors, the resistances of which may be set by values entered into control register 380 (which may be implemented as a single or multiple registers). The processor with which the circuit of Figure 3B may be integrated may set the values in control register 380 to control the output at 360.

In accordance with an embodiment of the present invention in which the circuit of Figure 3B is used as a local voltage regulator, a stable reference voltage, Vref, may be provided as input voltage 365. Vcc(global) may be provided as supply voltage 355, and Vcc(local) may be provided at output 360. Vcc(local) at output 360 may be determined by the equation Vref x (1+ 375/370), where 375 and 370 are the resistances of resistors 375 and 370, respectively.

In accordance with one embodiment of the present invention, one or more voltage regulators of a processor may include one or more op amps, e.g. as described above, to provide one or more local supply voltages. One or more voltage regulators of a processor may alternatively include one or more comparators, or switching regulators, separately or in addition to one or more op amps. For one embodiment of the present invention, Vcc(local) may be lower than

Vcc(global). For another embodiment, Vcc(local) may be greater than Vcc(global). For one embodiment of the present invention, a switch may be used as a pass element to source current for the voltage regulator to, for example, help reduce the size of the regulator.

Figure 4 includes a flow chart showing a method of the present invention. As shown at step 405, a global supply voltage, Vcc(global), may be provided to a global power grid of a processor from an external, discrete voltage regulator. At step 410, a first local supply voltage, Vcc(local), is provided to a first local power grid to power a first circuit of the processor. This first Vcc(local) is set high enough to allow the first circuit to meet a timing requirement. At step 415, a second local supply voltage, Vcc(local), is provided to a second local power grid to power a second circuit of the processor. This second Vcc(local) is set high enough to allow the second circuit to meet a timing requirement. Note that the first and second local supply voltages may be set to different values and may be adjusted independently of each other.

At step 420 of Figure 4 it is determined if the first circuit is inactive. If the first circuit is inactive, then the local supply voltage to the first circuit is reduced at step 425. Next, at step 430 it is determined if the second circuit is inactive. If the second circuit is inactive, then the local supply voltage to the second circuit is reduced at step 435.

This invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident to persons having the benefit of this disclosure that various modifications and changes may be made to these embodiments without departing from the broader spirit and scope of the invention.

The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

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